PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Akram et al.

Serial No.: 10/033,234

Filed: December 28, 2001

For: MULTI-CHIP MODULE SYSTEM AND METHOD OF FABRICATION

Examiner: David E. Graybill

Group Art Unit: 2827

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AMENDMENT

Box NON-FEE AMENDMENT
Commissioner for Patents
Washington, D.C. 20231

Sir:

This amendment is in response to the Office Action of August 14, 2002, whose initial period of response is set to expire on November 14, 2002.

IN THE CLAIMS:

Please note that all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity.

Please amend the claims as follows:

1. A method of manufacturing a multichip module system comprising:
forming a substrate for use in said multichip module system, said substrate having at least a first position for locating a first semiconductor device thereat and having at least one other vacant position for locating a second semiconductor device thereat on said substrate;
installing said first semiconductor device in the at least a first position of the substrate;
determining if the multichip module system has an unacceptable semiconductor device; and
repairing the substrate to have an acceptable semiconductor device by installing a second semiconductor device in the at least one other vacant position in the substrate.

2. The method of claim 1, further comprising:
installing a known-good-die in the at least one other vacant position on the substrate for use in said multichip module system.

3. The method of claim 1, further comprising:
testing said multichip module system for compliance with predetermined operational characteristics for the second semiconductor device.

4. The method as defined in claim 1, further comprising:
repairing the substrate for use in said multichip module system to have said acceptable semiconductor device thereon by installing said second semiconductor device having an adapter attached thereto, the adapter having to be operably installed in the at least one other vacant position in the substrate.

5. The method of claim 4, further comprising:

installing a known-good-die having said adapter attached thereto, the adapter to be operably installed in the at least one other vacant position in the substrate for use in said multichip module system as the second semiconductor device.

6. The method as defined in claim 5, further comprising:

testing said multichip module system to ensure compliance with predetermined operational characteristics for the second semiconductor device.

7. A method of manufacturing a multichip module system comprising:

forming a substrate for use in said multichip module system, the substrate having at least a first position for locating a first semiconductor device thereat and having at least one other vacant position for locating a second semiconductor device thereat on the substrate;

installing said first semiconductor device in the at least a first position of the substrate;

determining if the multichip module system has an unacceptable semiconductor device; and

repairing the substrate to have an acceptable semiconductor device by installing said second semiconductor device in the at least one other vacant position in the substrate, the second semiconductor device comprising a known-good-die.

8. The method of claim 7, further comprising:

testing said multichip module system to ensure compliance with predetermined operational characteristics for the second semiconductor device.

9. A method of manufacturing a multichip module system comprising:

forming a substrate for use in said multichip module system, the substrate having at least a first position for locating a first semiconductor device thereat and having at least one other vacant position for locating a second semiconductor device thereat on the substrate;

installing said first semiconductor device in the at least a first position of the substrate;

determining if the multichip module system has an unacceptable semiconductor device; and

repairing the substrate to have an acceptable semiconductor device thereon by installing said second semiconductor device having an adapter attached thereto, the adapter to be operably installed in the at least one other vacant position in the substrate.

10. The method of claim 9, further comprising:

installing a known-good-die having said adapter attached thereto, the adapter having to be operably installed in the at least one other vacant position in the substrate for use in said multichip module system as the second semiconductor device.

11. The method as defined in claim 10, further comprising:

testing said multichip module system for compliance with predetermined operational characteristics for the second semiconductor device.

12. A method of manufacturing a multichip module system comprising:

forming a substrate for use in said multichip module system, the substrate having at least first and second positions thereon, the at least first and second positions for locating a first and second semiconductor device thereat, and having at least one other vacant position for locating a third semiconductor device thereat on the substrate;

installing said first and second semiconductor devices in the respective at least first and second positions of the substrate, the first and second semiconductor devices each having the same predetermined performance capability;

determining if the multichip module system has an unacceptable semiconductor device thereon;

disabling circuitry connected to the unacceptable semiconductor device; and

repairing the substrate to have an acceptable semiconductor device thereon by installing a third semiconductor device in the at least one other vacant position in the substrate, the third semiconductor device installed in the at least one other vacant position having said predetermined performance capability.

13. The method of claim 12, further comprising:
removing the unacceptable semiconductor device from the substrate.

14. A method of manufacturing a multichip module system comprising:
forming a substrate for use in said multichip module system, said substrate having at least first and second positions for locating a first and second semiconductor device thereat, and having at least one other vacant position for locating a third semiconductor device thereat;
installing a first and second semiconductor device in said respective first and second positions of said substrate, said first and second semiconductor devices each having a predetermined performance capability;
determining if said multichip module system has an unacceptable semiconductor device thereon;
disabling circuitry connected to said unacceptable semiconductor device; and
repairing said substrate to have an acceptable semiconductor device thereon by installing said third semiconductor device in said at least one other vacant position in said substrate, said third semiconductor device installed in said at least one other vacant position having a predetermined performance capability, said third semiconductor device comprising a known-good-die having a predetermined performance capability.

15. The method of claim 14, further comprising:
testing said multichip module system for compliance with said predetermined performance capability for said third semiconductor device.

16. The method of claim 15, further comprising:
repairing said substrate for use in said multichip module system to have said acceptable semiconductor device thereon by installing said third semiconductor device in said at least one other vacant position in said substrate, said third semiconductor device installed in said at least one other vacant position having said predetermined performance capability of a combined predetermined performance capability of said first and the second semiconductor device.

17. A method of manufacturing a multichip module system comprising:

forming a substrate for use in said multichip module system, said substrate having at least first and second positions thereon, said first and second positions each for locating a first and second semiconductor device thereat, and having at least one other vacant position for locating a third semiconductor device thereat on said substrate;

installing a first and second semiconductor device in said respective first and second positions of said substrate, said first and second semiconductor devices each having a predetermined performance capability;

determining if said multichip module system has an unacceptable semiconductor device thereon;

disabling circuitry connected to said unacceptable semiconductor device; and

repairing said substrate to have an acceptable semiconductor device thereon by installing said third semiconductor device having an adapter attached thereto, said adapter for installation in said at least one other vacant position in said substrate.

18. The method of claim 17, further comprising:

installing a known-good-die as said third semiconductor device having said adapter attached thereto, said adapter for installation in said at least one other vacant position in said substrate for use in said multichip module system as said third semiconductor device.

19. The method as defined in claim 18, further comprising:

testing said multichip module system for compliance of said third semiconductor device with a predetermined performance capability for said third semiconductor device.

20. The method of claim 17, further comprising:

forming said substrate for use in said multichip module system, said substrate having at least a first position having a first mounting configuration for a semiconductor device thereat, having a second position having a second mounting configuration for a semiconductor device thereat different than said first mounting configuration, and having said at least

one other vacant position having, in turn, a predetermined configuration for locating said third semiconductor device thereat on said multichip module system.

21. The method of claim 20, further comprising:

configuring one other vacant position located on said substrate to have a predetermined semiconductor mounting configuration for corresponding to said first mounting configuration of said first semiconductor device and for corresponding to said second mounting configuration of said second semiconductor device.

22. The method of claim 21, further comprising:

configuring said location of said one other vacant position located on said substrate such that on one side of said substrate said one other vacant position has said predetermined semiconductor mounting configuration which corresponds to said first mounting configuration of said first semiconductor device; and

forming on an other side of said substrate a second vacant position that has a predetermined configuration for corresponding to said second mounting configuration of said second semiconductor device.

23. A method of manufacturing a multichip module system comprising:

forming a substrate for use in said multichip module system, said substrate having at least a first position for a semiconductor device to be located thereat, having a second position having a second mounting for a semiconductor device to be located thereat different than said at least said first position, and having at least one other vacant position for locating a third semiconductor device thereat on said multichip module system;

installing a first semiconductor device in said at least said first position of said substrate;

determining if said multichip module system has an unacceptable semiconductor device thereon;

disabling said circuitry connected to said unacceptable semiconductor device; and

repairing said substrate to have an acceptable semiconductor device thereon by installing a second semiconductor device in said at least one other vacant position in said substrate.

24. The method of claim 23, further comprising:

wherein said third semiconductor device includes a known-good-die in said at least one other vacant position on said substrate for use in said multichip module system.

25. The method as defined in claim 23, further comprising:

configuring said at least one other vacant position located on said substrate to have a predetermined semiconductor mounting configuration for corresponding to a first mounting configuration of said first semiconductor device and for corresponding to said second mounting of said second semiconductor device.

26. The method of claim 23, further comprising:

removing said unacceptable semiconductor device from said substrate.

27. The method of claim 23, further comprising:

configuring said location of said at least one other vacant position located on said substrate such that on one side of said substrate said at least one other vacant position has a predetermined semiconductor mounting configuration for corresponding to said first semiconductor device; and

forming on an other side of said substrate a second vacant position that has a predetermined configuration for corresponding to said second mounting of said second semiconductor device.

28. The method of claim 23, further comprising:

installing a third semiconductor chip in said at least one other vacant location, said third semiconductor chip having a predetermined mounting configuration for corresponding to said first semiconductor device.

29. The method of claim 23, further comprising:

installing a third semiconductor chip in said at least one other vacant location, said third semiconductor chip having a predetermined mounting configuration for corresponding to the second mounting of said second semiconductor device.

30. The method of claim 27, further comprising:

installing a third semiconductor chip in said at least one other vacant location on said one side of said substrate, said third semiconductor chip having said predetermined mounting configuration for corresponding to said first semiconductor device.

31. The method of claim 27, further comprising:

installing a third semiconductor chip in said second vacant location on said other side of said substrate, said third semiconductor chip having a predetermined mounting configuration for corresponding to said second mounting configuration of said second semiconductor device.

32. The method of claim 31, further comprising:

disabling circuitry connected to said unacceptable semiconductor device.

33. The method of claim 31, further comprising:

removing said unacceptable semiconductor device from said substrate.

34. A method of manufacturing a multichip module system comprising:

forming a substrate for use in said multichip module system, said substrate having at least a first position for locating a semiconductor device thereat, having a second position having a second mounting configuration for locating a semiconductor device thereat different than said at least said first position, having at least a first vacant position having, in turn, a third configuration for locating a third semiconductor device thereat on said substrate, and having a second vacant position having, in turn, a fourth configuration for locating a fourth semiconductor device thereat on said substrate;

installing a first semiconductor device in said at least said first position of said substrate, said first semiconductor device having a first performance capability;

installing a second semiconductor device in said second position of said substrate, said second semiconductor device having a second performance capability;

determining if said multichip module system contains an unacceptable semiconductor device thereon;

determining if said unacceptable semiconductor device is said first semiconductor device;

configuring said at least said first vacant position located on said substrate to have a third semiconductor mounting configuration for corresponding to said at least said first position of said first semiconductor device;

configuring said second vacant position located on said substrate to have a fourth semiconductor configuration for corresponding to said second mounting configuration of said second semiconductor device; and

installing said third semiconductor device having a performance capability of said unacceptable semiconductor device in one of said at least said first vacant position or said second vacant position.

35. The method of claim 34, further comprising:

configuring said second vacant position located on said substrate to have a fourth predetermined semiconductor configuration for corresponding to said second mounting configuration of said second semiconductor device.

36. The method of claim 34, further comprising:

configuring said location of said at least said first vacant position to be located on said substrate on one side thereof such that said one side of said substrate has said at least said first vacant position thereon having a third predetermined semiconductor mounting configuration for corresponding to a first predetermined mounting configuration of said first semiconductor device; and

configuring said location of said second vacant position to be located on an other side of said substrate such that said second vacant position has a fourth predetermined configuration for corresponding to said second mounting configuration of said second semiconductor device.

37. The method of claim 34, further comprising:

installing said third semiconductor device having a performance capability of said first semiconductor device if said first semiconductor device is determined to be unacceptable.

38. The method of claim 34, further comprising:

determining if said unacceptable semiconductor device is said second semiconductor device.

39. The method of claim 38, further comprising:

installing a fourth semiconductor device having a performance capability of said second semiconductor device if said second semiconductor device is determined to be unacceptable.

40. The method of claim 34, further comprising:

removing said unacceptable semiconductor device from said substrate.

41. The method of claim 34, further comprising:

disabling the circuitry connected to the unacceptable semiconductor device.

REMARKS

Claims 1 through 41 are currently pending in the application.

This amendment is in response to the Office Action of August 14, 2002.

Claims 37 and 39 stand rejected under 35 U.S.C. 101 as being directed to non-statutory subject matter in that they are drawn to an abstract idea. In particular, the language "if said first semiconductor die is determined to be unacceptable" in claim 37 and "if said second semiconductor device is determined to be unacceptable" in claim39 is said to be abstract in that it does not require an action to be taken. However, the fact that a set of procedural steps bifurcates at the performance of a certain type of act and the determination of a certain result does not make the procedure abstract. The act of performing the determination is but a step in the process. Furthermore, the fact that the claim language requires a judgment according to a set of standards not given detailed disclosed in the specification does not necessarily mean the process is abstract. Applicants' disclosure and claims are a case in point. Applicants have invented, among other things, a method for avoiding the disruption to a semiconductor-device-bearing substrate caused by the removal and replacement of a semiconductor device which has been determined to be functioning unsatisfactorily. Specification paragraphs [0007] and paragraph [0029].The standard for determining whether or not a device is functioning in a satisfactory manner could be seen as immaterial to the invention. Finally, as set forth below, Applicants respectfully assert that the fact that Applicants method requires the determination step to take place in the presence of a vacancy is enough to support patentability, regardless of the standard for satisfactory functioning or the outcome of the decision whether or not to replace the semiconductor device..

Claims 12, 13, 16, and 34 through 41 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicant understands the Examiner's position to be that because Applicant does not fully detail in the specification the level of "performance capability" that gives an "unacceptable" semiconductor device, Applicants do not meet the foregoing standard. However, similarly to the argument above, the patentability of Applicants' claims could be seen as independent of such a judgment. The practitioner can benefit from the efficiencies of building a vacancy into the substrate regardless of his standards for an acceptable semiconductor device

Claims 12 through 41 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Claims 21, 22, 25, 27-31 and 34 through 36 are rejected in that the meaning of the phrase "configuration corresponding to" is ambiguous. The specification does not give a detailed definition of the term. However, in a manner similar to the argument above, Applicants respectfully assert that the patentability of the claims is independent of the wide scope which can be given to the phrase.

Claims 12, 13, as well as claims 14, 17 through 23, 26, 32, 32, 38, 40 and 41 are rejected for insufficient antecedent basis for the phrases "the unacceptable semiconductor device" and "said unacceptable semiconductor device," respectively. However, each independent claim contains the phrase "determining if the multichip module has an unacceptable semiconductor device thereon."

Claim 16 is rejected for having insufficient antecedent basis for the phrase "said predetermined performance capability of a combined predetermined performance capability of said first and the second semiconductor device." Applicants respectfully submit that the phrase is a property of the "third semiconductor device" mentioned earlier in the claim, and thus the first "said" in the claim refers to the "predetermined performance capability" given to the third semiconductor device in the end of claim 14.

Claim 12 is rejected because there is "ambiguous and insufficient antecedent basis for the language, 'said predetermined performance capability.'" It has been duly amended to reflect the

fact that the first and second semiconductor devices each have the same predetermined performance capability.

Claims 1 through 3, 7, 8, 12 through 15, and 23 through 41 were rejected under 35 U.S.C. § 102(b) as being anticipated by Corbett (United States Patent 4,992,850). A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants respectfully submit that Corbett does not disclose a process which contains all of the elements of Applicant's claims, the volume of cited material notwithstanding. The rejected claims all contain, among other things, three steps, performed in a specific order. These steps require that 1) one or more vacancies be created on a substrate, the substrate also containing at least one semiconductor device; 2) the semiconductor devices on the substrate are tested for functionality, usually by burn-in, functional testing, or other testing, in the presence of the vacancy; 3) installment, in the one or more vacancies, of additional dice to compensate for non-functioning devices. Corbett cannot be read to teach the running or testing of a circuit containing a vacancy. Corbett also cannot be read to teach the installment of an additional die in the vacancy after determination of the existence of non-functional semiconductor devices. As a matter of fact, Corbett actually recommends replacement of failed dice. Col 6, line 68; Col 7, line 1. From the absence of any language indicating the presence of a vacancy, it is clear that Corbett contemplates removal of the non-functioning dice, with any vacancy being created *after* the determination that one or more of the semiconductor devices is non-functional. Applicant respectfully submits that claims1 through 3, 7, 8, 12 through 15 and 23 through 41 are not anticipated by Corbett because Corbett does not describe, either expressly or inherently, all the claim elements of the invention in an identical manner as the claimed invention. Therefore, such claims are allowable.

Claims 4 through 6, 9 through 11, and 17 through 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Corbett (United States Patent 4,992,850) as applied to claims 1 through 3, 7, 8, 12 through 15, and 23 through 41 above, and further in combination with Derouiche (United States Patent 5,623,395). Applicants submit that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

The combination of Corbett with Derouiche fails to teach every limitation of Applicants claimed invention to establish a *prima case* of obviousness under 35 U.S.C. § 103. As set forth above, Corbett fails to teach 1) the determination of failed semiconductor devices on a substrate with one or more vacancies, and 2) the installation of one or more additional semiconductor devices in the one or more vacancies, wherein the vacancies exist at the time of testing. Derouiche fails to teach these elements as well, and thus the combination of the two references does not teach every element of Applicants' claimed invention to establish a *prima* facie case of obviousness under 35 U.S.C. § 103.

Claims 1 through 34 and 36 through 41 stand rejected under 35 U.S.C. § 101 as claiming the same invention as that of claims 1 through 40 of prior United States Patent 5,807,762. Claims 1 through 41 stand rejected under 35 U.S.C. § 101 as claiming the same invention as that of claims 1 through 41 of prior United states Patent 6,395,565. Applicants respectfully traverse both rejections, as hereinafter set forth.

Applicants' claimed invention of the present application are claiming a different embodiment of the invention than that of the `565 patent or the `762 patent. Claim1 of '762 requires forming a substrate "having at least a first position having, in turn, a predetermined

configuration for locating a first semiconductor device thereat," as well as "a least one other vacant position having, in turn, a predetermined configuration for locating a second semiconductor device thereat on the substrate." Applicants claimed embodiment of the invention recites a substrate "having at least a first position for locating a first semiconductor device thereat, and having at least one other vacant position for locating a second semiconductor device thereat on said substrate." While the embodiment of the claimed invention may appear similar in form, the "predetermined configuration" is a limitation contained in the cited prior patents which narrows the embodiment of the invention claimed therein in comparison to Applicants' claims.

There exist areas of subject matter which are outside the scope of the cited art's claims, but inside the scope of Applicants' claims. Applicants' claimed embodiment of the invention is, among other things, a method for eliminating the need to remove and replace failed semiconductor devices. The method involves building one or more vacant connections into the substrate. Upon device failure, another device of the same type as the failed device is connected to the vacancy to compensate for the failed device. However, if a substrate has two or more different types of semiconductor devices on it., configuring a vacancy to accept one type of semiconductor device may limit the ability to use the vacancy to compensate for the failings of another type of semiconductor device on the board. The scope of the embodiments of the Applicants' claimed invention is intended to encompass such a situation. The specification describes a situation in which the vacancy is not provided with electrical connections until after device failure in paragraph [0035].

Applicants' claimed embodiments of inventions have a different scope than the '565 patent. Claim 1 of the '565 patent reads similarly to the '762 patent, but omits the word "predetermined." Thus, the embodiments of Applicants claimed inventions clearly extend beyond the scope of these embodiments of the claimed inventions in that Applicants' embodiments of the claimed inventions encompass the instance in which the vacancy is not yet configured or only partially configured.

Claims 2 through 6 are respectfully deemed allowable as depending from Claim1. Claims 4 and 5 also set forth an embodiment of the claimed invention calling for , unlike both pieces of cited art, the adapter need not have a "predetermined configuration." Thus, Applicants' embodiments of the claimed inventions encompass, for example, the case in which the vacancy is not configured, but can more easily be configured to accept the adapter than the semiconductor device itself.

Independent claims 7, 9, 12, 14, 17, 23 and 34 of both pieces of cited art can be compared to Applicants' analogous claims in a manner similar to the way claim 1 is compared above. Claims 8; 10, 11; 13; 15, 16, 20; 18-19; 20 through 22; 24 through 33 and 35 through 41 are respectfully deemed allowable as dependent from allowable claims 7, 9, 12, 14, 17, 23 and 34 respectively. In addition, claim 11 is deemed allowable for substantially the same reason as claims 4 and 5.

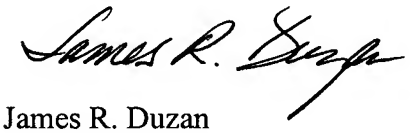
Independent claims 12, 14 and 17 have additional embodiments of the invention claimed in that their scopes encompass the instances in which the third device, though a known-good-die, is not operable after installation.

It is respectfully submitted that because the embodiments of the Applicant's claimed invention is not identical to the embodiments of the claimed inventions of the '565 and '762 patents, the statutory double-patenting rejection based on 35 U.S.C. 101 is improper.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants submit that claims 1 through 41 are clearly allowable.

Applicants request the allowance of claims 1 through 41 and the case passed for issue.

Respectfully submitted,



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Enclosure: Version with Markings to Show Changes Made

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